Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-7. (canceled)

8. (currently amended) A method for fabricating a CMOS semiconductor device structure comprising gate electrodes, said method comprising:

providing a dielectric layer on a substrate;

depositing a hafnium nitride layer on said dielectric layer wherein an atomic ratio of Nitrogen and Hafnium of said hafnium nitride layer is adjusted to adjust the work-function of said gate electrodes wherein said atomic ratio of nitrogen to hafnium remains greater than ~~or equal to~~ one;

depositing a capping layer on said hafnium nitride layer;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form said CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

9. (original) The method according to Claim 8 wherein said depositing of said hafnium nitride layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target.

10 . (original) The method according to claim 9 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

11. (previously presented) The method according to Claim 8 wherein said dielectric layer comprises HfO_2 and is deposited at 400°C using a MOCVD cluster tool.

12. (previously presented) The method according to Claim 8 wherein said dielectric layer comprises HfO_2 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in a N_2 ambient.

13. (canceled)

14. (previously presented) The method according to Claim 8 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

15. (original) The method according to Claim 8 further comprising thermal treatment of said hafnium nitride layer by rapid thermal annealing (RTA) at about 1000 °C for about 20 seconds.

16-23. (canceled)

24. (currently amended) A method for fabricating a CMOS semiconductor device structure comprising gate electrodes, said method comprising:

providing a dielectric layer on a substrate;

depositing a first metal layer on said dielectric layer wherein said depositing of said first metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form a hafnium nitride layer as a first metal layer and wherein an atomic ratio of Nitrogen and Hafnium of said hafnium nitride layer is adjusted to adjust the work-function of said gate electrodes wherein said atomic ratio of nitrogen to hafnium remains greater than ~~or equal to~~ one;

depositing a second metal capping layer on said first metal layer wherein said second metal is different from said first metal;

patterning said second metal capping layer, said first metal layer, and said dielectric layer to form said CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

25. (canceled)

26. (previously presented) The method according to Claim 24 wherein said second metal capping layer comprises tungsten or tantalum nitride.

27. (original) The method according to Claim 24 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition.

28-34. (canceled)

35. (currently amended) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a hafnium nitride layer on said dielectric layer wherein said depositing comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target and wherein an atomic ratio of Nitrogen and Hafnium of said hafnium nitride layer is adjusted to adjust the work-function of said gate electrodes wherein said atomic ratio of nitrogen to hafnium remains greater than one;

depositing a titanium nitride or tungsten capping layer on said hafnium nitride layer;

patterning said hafnium nitride layer and said capping layer and said dielectric layer to form CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

36. (canceled)

37. (previously presented) The method according to Claim 35 wherein said dielectric layer comprises HfO_2, silicon dioxide, silicon nitride, nitrided silicon dioxide, zirconium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, or crystalline oxides.

38. (canceled)

39. (previously presented) The method according to Claim 35 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

40. (previously presented) A method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer on a substrate;

depositing a first metal layer on said dielectric layer;

depositing a second metal capping layer on said first metal layer wherein said depositing comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form said second metal capping layer comprising hafnium nitride;

patterning said first metal layer, said second metal capping layer, and said dielectric layer to form CMOS gate electrodes; and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

41. (previously presented) The method according to Claim 40 wherein said dielectric layer comprises HfO_2.

42. (previously presented) The method according to Claim 40 wherein said first and second metal layers are deposited by physical vapor deposition or chemical vapor deposition.

43. (previously presented) The method according to Claim 40 wherein said first metal layer comprises tungsten or tantalum nitride.

44. (canceled)

45. (previously presented) The method according to Claim 40 further comprising adjusting the flow rate of said Nitrogen and Argon atoms to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium remains greater than or equal to one.

46. (previously presented) The method according to Claim 40 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

47. (currently amended) The method according to Claim 40 further comprising thermal treatment of said hafnium nitride layer by rapid thermal annealing (RTA) at about 1000 °C for about 20 seconds.

48-53. (canceled)

54 . (previously presented) The method according to claim 24 wherein argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

55. (previously presented) The method according to Claim 24 wherein said dielectric layer comprises HfO_2 and is deposited at 400°C using a MOCVD cluster tool.

56. (previously presented) The method according to Claim 24 wherein said dielectric layer comprises HfO_2 and wherein said dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in a N_2 ambient.

57. (canceled)

58. (previously presented) The method according to Claim 24 further comprising impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

59. (currently amended) The method according to Claim 24 further comprising thermal treatment of said hafnium nitride layer by rapid thermal annealing (RTA) at about 1000 °C for about 20 seconds.